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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re application of:

Kalnitsky *et al.*

Serial No. 08/163,043

Filed: 12/06/93

: Art Unit:

: Examiner:

: Atty's Docket: SGS-011/93-C-32

NOV 10 1994

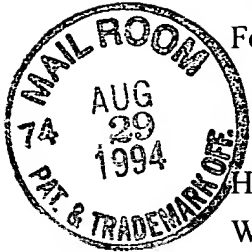
GROUP 1100

For: Enhanced Planarization Technique for an Integrated Circuit

INFORMATION DISCLOSURE STATEMENT

Honorable Commissioner of Patents and Trademarks

Washington, DC 20231



Sir:

The accompanying form PTO-1449 lists one or more documents which may be considered material to the examination of this application. A copy of each document is provided, if available.

Applicant reserves the right to establish the patentability of the claimed invention over any of the listed documents should they be applied thereagainst as references, and/or to prove that some of these documents may not be prior art, may not be within an analogous field of art, and/or may not be enabling for the teachings they purport to offer.

This statement should not be construed as a representation that an exhaustive search has been made, nor that more material information does not exist.

The Examiner is specifically requested to conduct an independent and thorough review of the documents, and to form his own opinions as to the significance of those documents to patentability of the claimed inventions, regardless of any of the foregoing statements concerning the significance of the references. The foregoing statements are made in good faith, and in compliance with the duty of disclosure; but they cannot substitute for the Examiner's specialized expertise, nor are they intended to derogate from the Examiner's official duty to assess patentability.

It is also respectfully noted that the submission of this material is not intended to displace the Examiner's professional ability and duty to search. Indeed, the Examiner is specifically requested not to rely on the materials submitted herewith, but to conduct a full independent search.

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It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449, to indicate in the file of this patent application that the documents have been considered.

Respectfully submitted,



Robert Groover, Reg.No. 30,059
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214-490-5335

Date: August 24, 1994



Robert Groover
Reg'd Patent Att'y

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GROUP 1100

Dr. Betty Formby,
Reg'd Patent Agent

August 24, 1994

Commissioner of Patents

Box Non Fee
Washington DC 20231

Re: Patent App'n SN
08/163,043 filed 12/06/93, of
Kalnitsky *et al.*, entitled
"Enhanced Planarization Technique for an Integrated Circuit" (Atty Docket No. SGS-011/93-C-32)

I certify that this correspondence, including the attachments listed, is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to Commissioner of Patents and Trademarks, Washington DC 20231, on the date shown below.

8-24-94
Date of Mailing



Signature of Person Mailing

Honorable Commissioner:

Enclosed is an Information Disclosure Statement (together with Form PTO-1449 and copies of cited references) in connection with the U.S. Patent Application referenced above. The correct amount of fee is believed to be as follows. A check for this amount is enclosed. Please charge any deficit or nonpayment, or credit any overpayment, to Deposit Account 07-2320. A duplicate copy of this sheet is enclosed.

<u>FEE CALCULATION</u>		
	Submission of IDS:	\$200
<u>Total Fee:</u>		<u>\$200</u>

Respectfully submitted,


Robert Groover, Reg.No. 30,059

Form PTO-1449

U.S. Dept. of Commerce
Patent & Trademark Office

Atty. Docket SGS-011/93-C-32

RECEIVED

SN 08/163,043

List of Documents
Cited by Applicant
(Use several sheets if necessary)Applicant: Kalnitsky *et al.*

NOV 10 1994

Filing Date: 12/06/93

GROUP 1100

Group:

U.S. PATENT DOCUMENTS

Ex'rs In'l		Document Number	Date	Name	Class	Sub- class	Filing Date, if applicable
	AA1	5,166,088		Ueda <i>et al.</i>			
	AB1	5,063,176		Lee <i>et al.</i>			
	AC1	4,824,767		Chambers <i>et al.</i>			
	AD1						
	AE1						
	AF1						
	AG1						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Sub- class	Trans'l'n Yes/No
-	AL1	327 412		EP			
	AM1						
	AN1						
	AO1						
	AP1						

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	AR1	J. Electrochem. Soc., Vol. 139, No. 2, 2/92, "Polysilicon Planarization Using Spin-On Glass", S. Ramaswami & A. Nagy, pgs 591-599.
	AS1	J. Electrochem. Soc., Vol. 139, No. 2, 2/92, "Three 'Low Dt' Options for Planarizing the Pre-metal Dielectric on an Advanced Double Poly BiCMOS Process", by W. Dauksher, M. Miller, and C. Tracy, pgs. 532-536.
	AT1	J. Electrochem. Soc., Vol. 140, No. 4, 2/93, "The Effect of Plasma Cure Temperature on Spin-On Glass", by H. Namatsu and K. Minegishi, pgs. 1121-1125.
	AU1	IEEE Electron Device Letters, Vol. 12, No. 3, 3/91, "Hot-Carrier Aging of the MOS Transistor in the Presence of Spin-on Glass as the Interlevel Dielectric", N. Lifshitz and G. Smolinsky, pgs. 140-142.

Examiner:

Date Considered:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PT0-1449		U.S. Dept. of Commerce Patent & Trademark Office		Atty. Docket SGS-011/93-C-32	
List of Documents Cited by Applicant (Use several sheets if necessary)		AUG 29 1994		RECEIVED SN 08/163,043	
				NOV 10 1994	
		Applicant: Kalnitsky <i>et al.</i>		Filing Date: 12/06/93	
				Group:	
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